IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2025

CIRCUITS AND SYSTEMS

Tuesday, 13 May 2025, 2:30PM

Time allowed: 2:00 hours

There are THREE questions on the paper.

Answer ALL questions.

Question 1 carries a weighting of 50%. The remaining questions carry a Weighting of 25% each.

Any special instructions for invigilators and information for Candidates are on page 1.

Examiners responsible First Marker(s): P.Y.K. Cheung

Second Marker(s): Aaron Zhao

Information for Candidates:

The following notation is used in this paper:

1. Unless explicitly indicated otherwise, digital circuits are drawn with their inputs on the left and their outputs on the right.
2. Within a circuit, signals with the same name are connected even if no connection is shown explicitly.
3. The notation X[2:0] denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.

1. (a) *Figure 1.1* shows an amplifier circuit using an op-amp operating at 3.3V and has a gain-bandwidth product of 1MHz. It amplifies the input signal V_S and produces an output voltage *Vout*.

(i) Derive from first principles the gain of this amplifier for both the DC and AC components of V_S. You must show your derivation clearly.

[4]

(ii) Given that V_S is a sine wave signal at 20kHz with a peak-to-peak voltage of 1V, sketch and explain the expected waveform at *Vout*.

[3]

(iii) State with justifications what happens to the gain of the amplifier if the frequency of V_S is changed to 1Hz and to 1MHz.

[3]

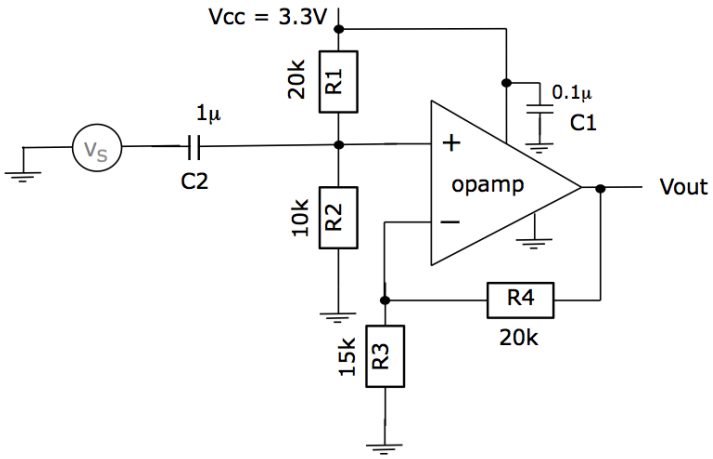


Figure 1.1

(b) *Figure 1.2* shows a 5-bit signature analyser circuit. FF1 to FF5 and G1 form a pseudo random number generator. G2 "merges" the input signal *in* with the random sequence to form a unique signature at the output Q[5:1]. The circuit is clocked by the clock signal *clk*. The output Q[5:1] is initialized synchronously to 5'b00001 if *init* is asserted.

(i) Assuming the input *in* is always zero and initially Q[5:1] = 5'b00001, list the first 6 values of Q[5:1] in the sequence.

[3]

(ii) The input instead of being always zero, it is in fact a sequence '010000'. What is the signature Q[5:1] after 6 clock cycles assuming the same initial condition as before?

[3]

(iii) Write a SystemVerilog module to implement this signature analyser.

[4]

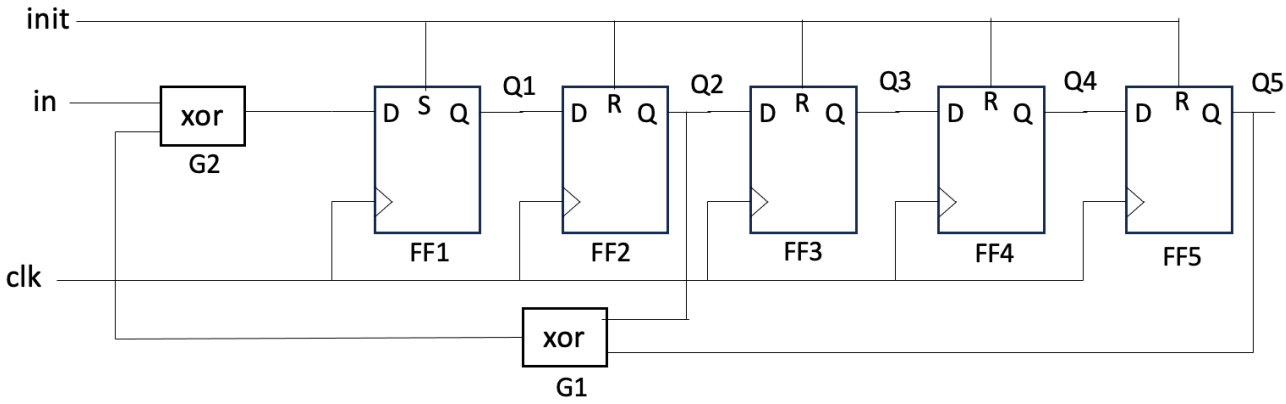


Figure 1.2

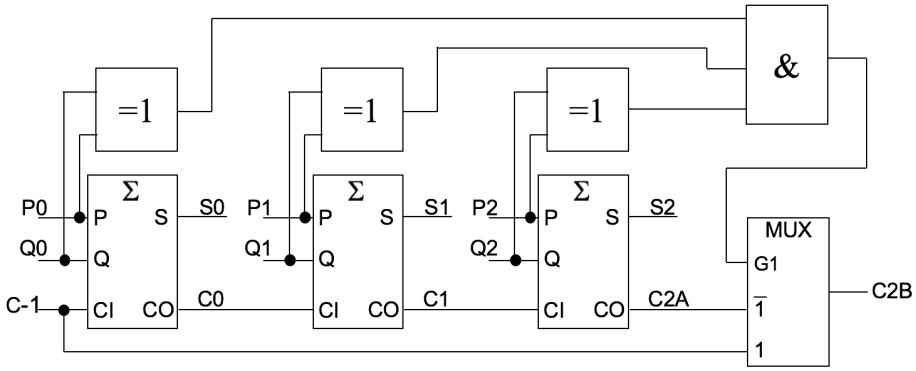
(c) *Figure 1.3(a)* shows the circuit of a 3-bit carry-skip binary adder. The worst-case propagation delays of the circuit elements are given in *Figure 1.3(b)* (in nanoseconds).

(i) Determine the worst-case propagation delays from P0 and from C_{-1} to C2A and C2B.

[6]

(ii) This adder is part of a pipeline stage in a digital system where registers have a setup time of 2ns, a hold time of 1ns and a clock to output delay of 1.5ns. If this binary adder is the combinational circuit with the worst-case delay, what is the maximum system clock frequency that can be deployed?

[4]



(a)

Device	Path	Delay
Adder	any input → S any input → CO	3 2
Multiplexer	SEL → output data input → output	3 2
XOR gate	any input → output	2
AND gate	any input → output	1

(b)

Figure 1.3

(d) *Figure 1.4* shows the state diagram of a finite state machine (FSM) with two input signals X and Y, and one output signal Z, driven with a clock signal CLK. RST input signal resets the FSM synchronously to state A. Changes in X and Y are synchronised on the falling edges of CLK; changes in state and Z are synchronised on the rising edges of CLK.

(i) Complete the timing diagram shown in *Figure 1.5* given that the FSM is initially in state A.

[4]

(ii) Specify in SystemVerilog a design of this FSM using binary state encoding.

[6]

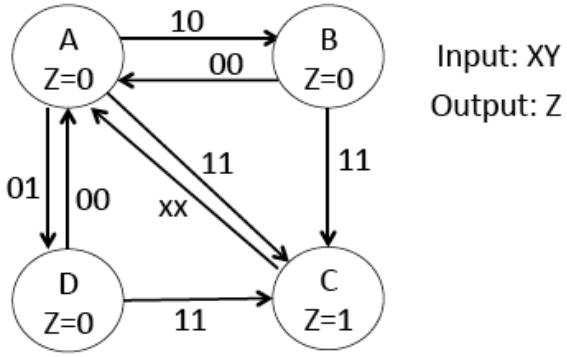


Figure 1.4

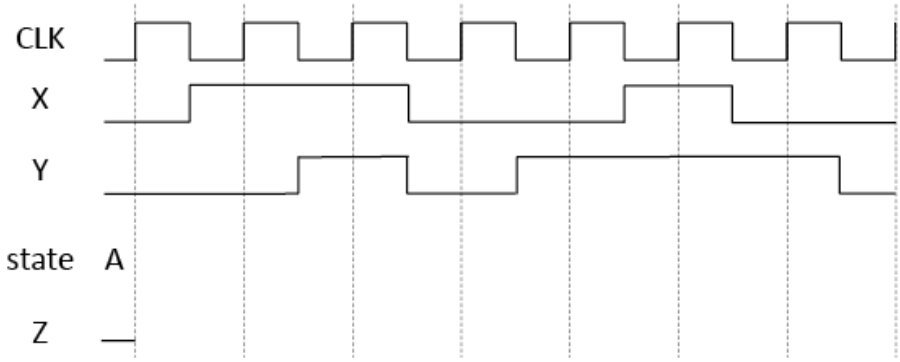


Figure 1.5

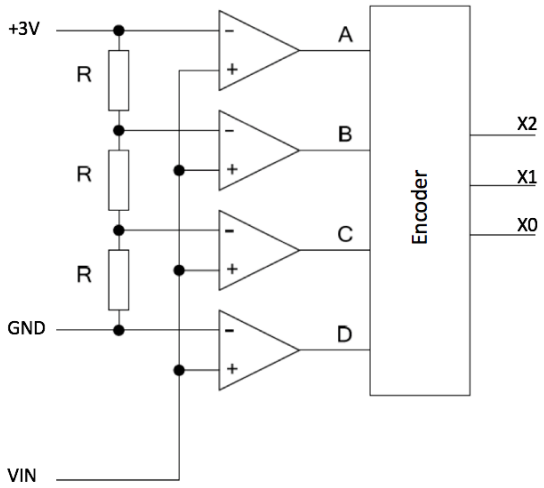
(e) *Figure 1.6(*a) shows a flash analogue-to-digital converter comprising three identical resistors, four comparators and a logic block. The output of a comparator is high whenever the voltage at the "+" input is greater than that at the "–" input. VIN is the analogue input to be converted. A, B, C and D are the outputs of the four comparators. X2:0 is the converted digital values for VIN.

(i) What are the ranges of voltage values of VIN for signals {A,B,C,D} to take on the values of 4'b0000, 4'b0001, 4'b0011, 4'b0111 and 4'b1111? State any assumptions used.

[5]

(ii) The truth table in *Figure 1.6(b)* defines the relationship between X2:0 and A, B, C and D of the encoder. Design the encode module in SystemVerilog.

[5]



(a)

ABCD	X2:0
0000	0
0001	1
0011	2
0111	3
1111	4

(b)

Figure 1.6

2. Part of the datasheet for the Microchip MCP6291 operational amplifier is included in the Appendix. Based on the information provided, answer the following questions with appropriate justifications.

(a) *Figure 2.1* shows MCP6291 is connected as an amplifier. If the input signal V_{IN} is a sinewave at 2.5MHz with an amplitude of 0.25V and a DC offset of 0.5V, what are the maximum and minimum voltages at the V_{OUT}? State any assumptions made.

[6]

(b) Sketch the output signal V_{OUT} if the input signal V_{IN} is a square wave signal at a frequency of 1MHz with low voltage at 0V and high voltage at 0.75V.

[4]

(c) *Figure 2.2* shows the MCP6291 connected as a light sensing amplifier. Given that the photodiode sensitivity characteristics are as shown and the irradiance E_θ is known to be 1mW/cm^2 or lower, what value of R should be used to provide the maximum voltage range at V_{OUT}?

[3]

(d) *Figure 2.3* shows a simplified SPICE model for the MCP6291 operational amplifier. The model has three parts: the input stage, the gain stage and the output stage. V+ and V- are the positive and negative power supplies to the operation amplifier respective. Based on the datasheet provided in the Appendix, answer the following questions:

(i) For the input stage, determine the values of R1, C1 and V1.

[2]

(ii) For the gain stage, determine the values of R2, C2 and the transconductance of G1.

[6]

(iii) Based on the values determined in part (ii) above, what is the SPICE statement for G1 which would model the slew rate for this operation amplifier?

[3]

(iv) What do D1 and D2 model?

[1]

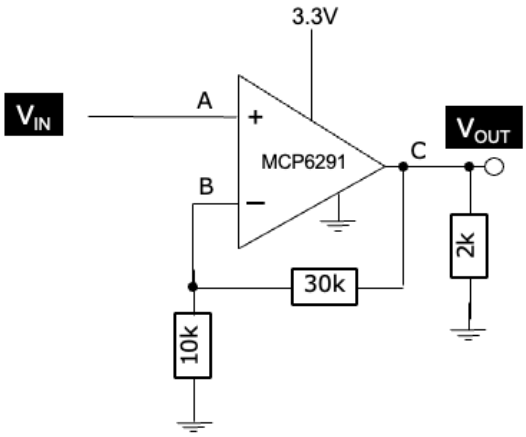


Figure 2.1

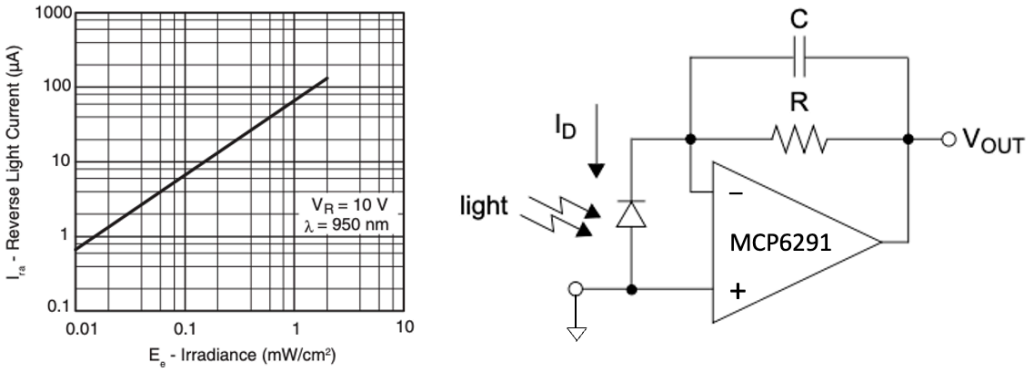


Figure 2.2

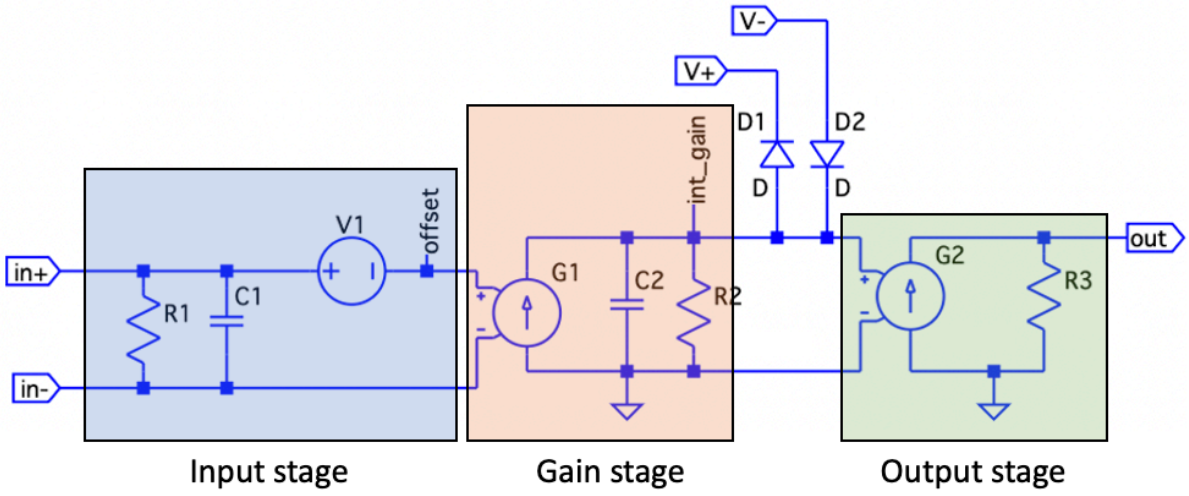


Figure 2.3

3. *Figure 3.1* shows a digital circuit that computes the approximate square root of a 10-bit number *P*[9:0] and produces a 5-bit answer *X*[4:0]. The circuit consists of a multiplier circuit, a digital comparator and a finite state machine that implements the successive approximation algorithm. The digital comparator output *GE* is high if the value at its input *A* is larger than or equal to its input *B*. The FSM is controlled by the clock signal *CLK*. It starts the computation when *LOAD* goes from low to high and the *DONE* signal then goes low until the computation is completed and *X*[4:0] contains the valid result.

(a) Given that *P*[9:0] = 10'h2A4, complete the timing diagram shown in *figure 3.2*.
[10]

(b) Hence or otherwise, explain how this circuit can compute the square root of the input *P*[9:0]. State any assumptions used.
[5]

(c) Design the SAR finite state machine in SystemVerilog.
[10]

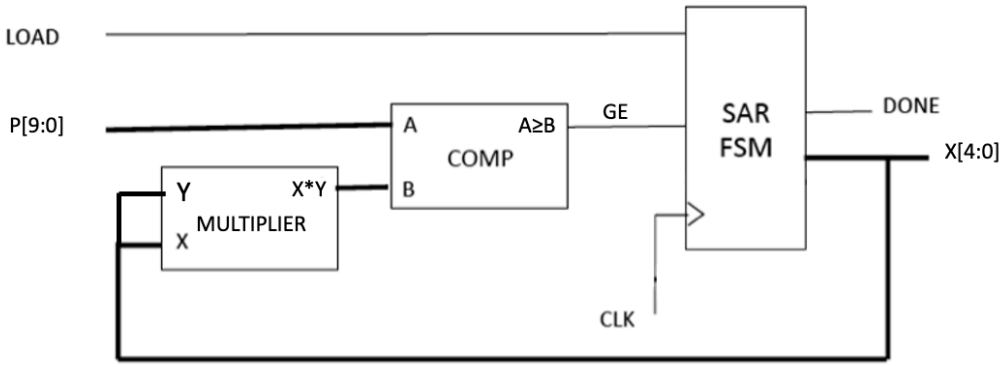


Figure 3.1

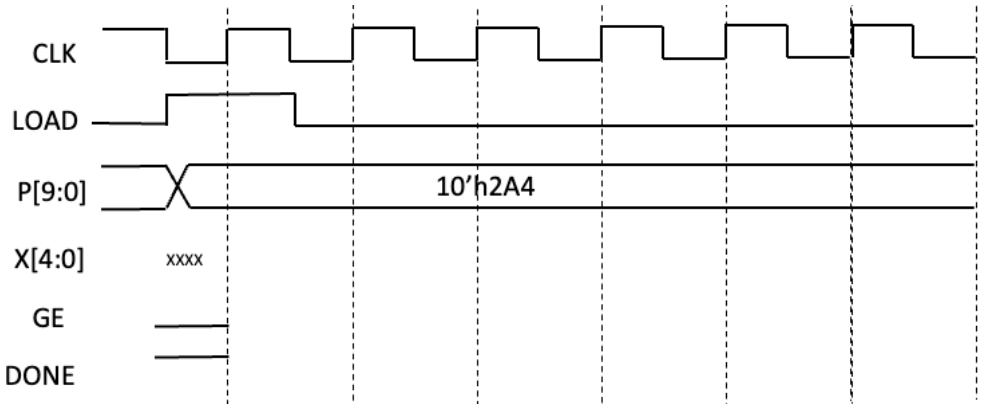


Figure 3.2

MCP6291/1R/2/3/4/5

1.0 mA, 10 MHz Rail-to-Rail Op Amp

Features

- Gain Bandwidth Product: 10 MHz (typical)
- Supply Current: I_Q = 1.0 mA
- Supply Voltage: 2.4V to 6.0V
- Rail-to-Rail Input/Output
- Extended Temperature Range: -40°C to +125°C
- Available in Single, Dual and Quad Packages
- Single with $\overline{CS}$ (**MCP6293**)
- Dual with $\overline{CS}$ (**MCP6295**)

Applications

- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Simulation Tool
- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

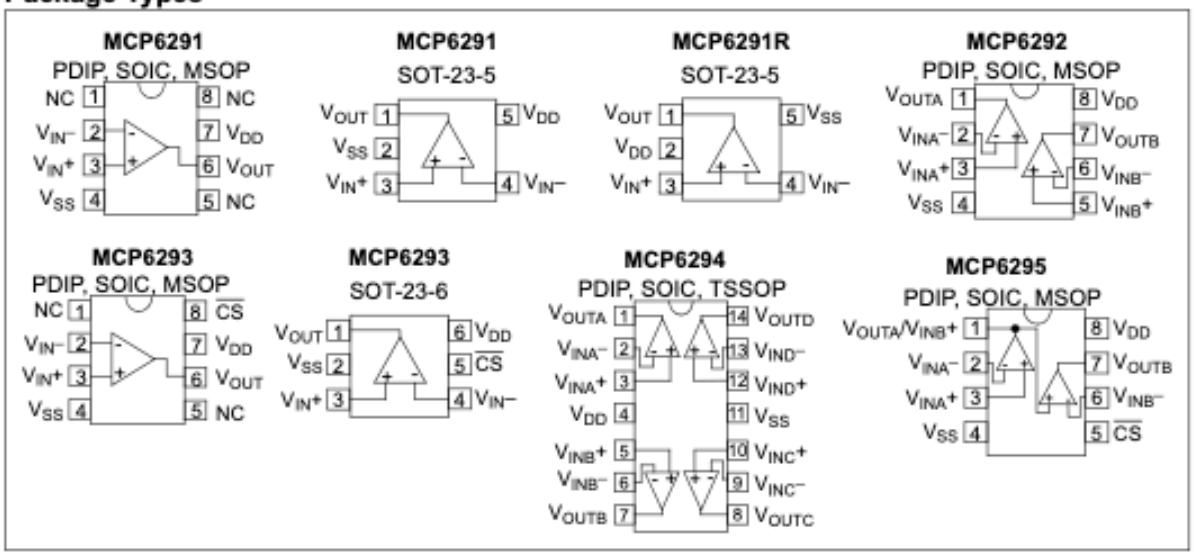
Description

The Microchip Technology Inc. MCP6291/1R/2/3/4/5 family of operational amplifiers (op amps) provide wide bandwidth for the current. This family has a 10 MHz Gain Bandwidth Product (GBWP) and a 65° phase margin. This family also operates from a single supply voltage as low as 2.4V, while drawing 1 mA (typical) quiescent current. In addition, the MCP6291/1R/2/3/4/5 supports rail-to-rail input and output swing, with a common mode input voltage range of V_{DD} + 300 mV to V_{SS} – 300 mV. This family of operational amplifiers is designed with Microchip's advanced CMOS process.

The MCP6295 has a Chip Select ($\overline{CS}$) input for dual op amps in an 8-pin package. This device is manufactured by cascading the two op amps, with the output of op amp A being connected to the non-inverting input of op amp B. The $\overline{CS}$ input puts the device in a Low-power mode.

The MCP6291/1R/2/3/4/5 family operates over the Extended Temperature Range of -40°C to +125°C. It also has a power supply range of 2.4V to 6.0V.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
Current at Input Pins .....±2 mA
Analog Inputs (V_{IN}+, V_{IN}–) †† ..... V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature.....–65°C to +150°C
Maximum Junction Temperature (T_J).....+150°C
ESD Protection On All Pins (HBM; MM) ..... ≥ 4 kV; 400V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**.

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.4V to +5.5V, V_{SS} = GND, $V_{OUT} \approx V_{DD}/2$, $V_{CM} = V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and $\overline{CS}$ is tied low (refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-3.0	—	+3.0	mV	$V_{CM} = V_{SS}$ **(Note 1)**
Input Offset Voltage (Extended Temperature)	V_{OS}	-5.0	—	+5.0	mV	T_A = -40°C to +125°C, $V_{CM} = V_{SS}$ **(Note 1)**
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	±1.7	—	µV/°C	T_A = -40°C to +125°C, $V_{CM} = V_{SS}$ **(Note 1)**
Power Supply Rejection Ratio	PSRR	70	90	—	dB	$V_{CM} = V_{SS}$ **(Note 1)**
Input Bias, Input Offset Current and Impedance						
Input Bias Current	I_B	—	±1.0	—	pA	**Note 2**
At Temperature	I_B	—	50	200	pA	T_A = +85°C **(Note 2)**
At Temperature	I_B	—	2	5	nA	T_A = +125°C **(Note 2)**
Input Offset Current	I_{OS}	—	±1.0	—	pA	**Note 3**
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	**Note 3**
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	**Note 3**
Common Mode (Note 4)						
Common Mode Input Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	
Common Mode Rejection Ratio	CMRR	70	85	—	dB	V_{CM} = -0.3V to 2.5V, V_{DD} = 5V
Common Mode Rejection Ratio	CMRR	65	80	—	dB	V_{CM} = -0.3V to 5.3V, V_{DD} = 5V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	90	110	—	dB	V_{OUT} = 0.2V to V_{DD} – 0.2V, $V_{CM} = V_{SS}$ **(Note 1)**
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 15	—	V_{DD} – 15	mV	0.5V Input Overdrive
Output Short Circuit Current	I_{SC}	—	±25	—	mA	
Power Supply						
Supply Voltage	V_{DD}	2.4	—	6.0	V	T_A = -40°C to +125°C **(Note 5)**
Quiescent Current per Amplifier	I_Q	0.7	1.0	1.3	mA	I_O = 0

Note 1: The MCP6295's V_{CM} for op amp B (pins V_{OUTA}/V_{INB}+ and V_{INB}–) is V_{SS} + 100 mV.
2: The current at the MCP6295's V_{INB}– pin is specified by I_B only.
3: This specification does not apply to the MCP6295's V_{OUTA}/V_{INB}+ pin.
4: The MCP6295's V_{INB}– pin (op amp B) has a common mode range (V_{CMR}) of V_{SS} + 100 mV to V_{DD} – 100 mV. The MCP6295's V_{OUTA}/V_{INB}+ pin (op amp B) has a voltage range specified by V_{OH} and V_{OL}.
5: All parts with date codes November 2007 and later have been screened to ensure operation at V_{DD} = 6.0V. However, the other minimum and maximum specifications are measured at 2.4V and or 5.5V.

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low (refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	10.0	—	MHz	
Phase Margin at Unity-Gain	PM	—	65	—	°	G = +1 V/V
Slew Rate	SR	—	7	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	4.2	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	8.7	—	nV/√Hz	f = 10 kHz
Input Noise Current Density	i_{ni}	—	3	—	fA/√Hz	f = 1 kHz

MCP6293/MCP6295 CHIP SELECT ($\overline{CS}$) SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low (refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	0.01	—	µA	$\overline{CS}$ = V_{SS}
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.7	2	µA	$\overline{CS}$ = V_{DD}
GND Current per Amplifier	I_{SS}	—	-0.7	—	µA	$\overline{CS}$ = V_{DD}
Amplifier Output Leakage	—	—	0.01	—	µA	$\overline{CS}$ = V_{DD}
Dynamic Specifications (Note 1)						
$\overline{CS}$ Low to Valid Amplifier Output, Turn-on Time	t_{ON}	—	4	10	µs	$\overline{CS}$ Low ≤ 0.2 V_{DD}, G = +1 V/V, V_{IN} = V_{DD}/2, V_{OUT} = 0.9 V_{DD}/2, V_{DD} = 5.0V
$\overline{CS}$ High to Amplifier Output High-Z	t_{OFF}	—	0.01	—	µs	$\overline{CS}$ High ≥ 0.8 V_{DD}, G = +1 V/V, V_{IN} = V_{DD}/2, V_{OUT} = 0.1 V_{DD}/2
Hysteresis	V_{HYST}	—	0.6	—	V	V_{DD} = 5V

Note 1: The input condition (V_{IN}) specified applies to both op amp A and B of the MCP6295. The dynamic specification is tested at the output of op amp B (V_{OUTB}).